Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

Applicants elect claim 1 for further prosecution in this application.

The new title better indicates the claimed matter.

The amended specification corrects an apparent typographical error.

Amended claim 1 and the new claims particularly point out and distinctly claim the subject matter the applicant regards as his invention, while presenting limitations that distinguish over the known art.

Claim 1 defines a process of selecting different 1149.1 TAP domain arrangements within an integrated circuit.

The process performs an 1149.1 instruction shift operation through a first 1149.1 TAP domain arrangement.

The process performs an 1149.1 instruction update operation at the end of said 1149.1 instruction shift operation.

In response to the 1149.1 instruction update operation, the process selects a second 1149.1 TAP domain arrangement that differs from the first 1149.1 TAP domain arrangement.

In contrast, US 6,311,302 to Cassetti, et al., discloses

an integrated circuit having core circuits 12 and 14 and a Chip Level TAP Linking Module CTLM 40. The portions of the patent relevant to the claimed inventions in the present application state:

A chip-level TLM 40 communicates with a common IEEE JTAG 1149.1 interface and with each of the multiple cores via the associated TLM register and two-part storage register. In accordance with certain embodiments of the present invention, the chip-level TLM 40 is also capable of using control signals to transfer control between the multiple cores. To accommodate this implementation, a TLM internal to one of the TLM'ed cores includes a storage unit that has both a TLM register adapted to store a decodable instruction, and a supplemental storage circuit adapted to store a coded signal. Control between the chip-level TLM and the cores 12 and 14 can be implemented, for example, using conventional IEEE JTAG 1149.1 signals, such as TMS, Capture, Shift and Update clock signals. In this specification, Capture clock is used to sample data in scan cells and is generated in a **CAPTURE-DR** state of the TAP state machine. Shift clock is used to shift data in scan cells and is generated in a **SHIFT-DR** state of the TAP state machine. Update clock is used to update the instruction register in the TLM 16 and is generated in an **UPDATE-DR** state of the TAP state machine.

In another example embodiment, each of the TAP controllers communicates with the chip-level TLM using such conventional control signals, and the TAP controllers operate as conventional TAP state machines, as defined in the IEEE JTAG 1149.1 specification. For example, when the TAP controller is in the **UPDATE-DR** state, the output of the TAP controller's data registers are latched to prevent changes at the parallel output while data is shifted in the associated shift-register path in response to certain instructions being received by the TAP controller. Further, in the **UPDATE-DR** state, the current instruction is not permitted to be changed until after this state is exited, which is upon the rising edge of TCK where the TAP controller enters either the select DR-Scan state if the TMS signal is held at 1 or the Run-Test/Idle state if the TMS signal is held at 0. These states and transitions are as characterized in IEEE Std. 1149.1-1990, and 1149.1-1993 (fully incorporated herein), and chapter five therein explains the operation of the TAP controller and illustrates the state machine for such a TAP controller. In this regard, reference may also be made to the above-referenced U.S. patent application Ser. No. 09/283,809 (VLSI.206PA). (column 4, line 53 to column 5, line 28)

The process begins, for example, at reset time when the internal TLM for the core 12 is active and the TAP controller 16 within it is enabled. Sometime after reset, the internal TLM for the core 14 is to be enabled and the internal TLM for the core 12 disabled. For this scenario, the TAP controller 16 selects the TLM register 20 and shifts in a value that sets the extension bit at 22. Since this extension bit is set, the TDI and TDO signals to the IC are now connected between the chip-level TLM 40 and the internal TLM for the core

12. In the next data loop, a command is shifted in the register internal to the chip-level TLM. At the end of the **Update DR** state for the TAP controller 16, the extension bit at 22 is cleared unconditionally. The new command thus shifted into the chip-level TLM 40 forces the TMS signal provided to the core 12 low, in turn forcing the TAP controllers 16 and 18 of the TLM'ed core 12 into IDLE state. At the same time, the TMS signal provided to the TLM'ed core 14 is enabled. (emphasis added, column 5, line 61 to column 6, line 10)

All the discussion in the Cassetti patent is specific to the data register scan protocol states. See Figure 2 of the present application for a depiction of the CAPTURE-DR, SHIFT-DR and UPDATE-DR states in the processes defined in IEEE 1149.1. Present claim 1 requires instruction shift and update scan protocol states.

The patent to Cassetti fails to disclose or suggest the limitations of present claim 1.

Applicant includes Information Disclosure Statement A.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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